MR-NAVQ95 PINOUT CHEAT SHEET

IO expansion board (MR-NAVQ95E-IO) **SHEET 1 / 2**

J22 GPS

JST-GH 1x10, side entry · DS-009 GPS · 3.3 V logic

1	5V out	VDD_CON_GPS_5V0		
2	UART5 TX	UART5_TX	GPIO_IO00	
3	UART5 RX	UART5_RX	GPIO_IO01	
4	I2C6 SCL	I2C6_SCL	GPIO_IO03	
5	I2C6 SDA	I2C6_SDA	GPIO_IO02	
6	Safety switch	ARM_IO	GPIO_IO07	
7	Safety LED	SW_LED_OUT	via PCAL6416 expander	I2C4 (GPIO_IO30/31)
8	3.3V out	VDD_CON_GPS_3V3		
9	Buzzer	BUZZER	via FET Q1	GPIO_IO23
10	GND			

9: enabled by DIP switch S1

J12 PWM

JST-GH 1x10, side entry · 3.3 V logic outputs

1	Servo rail	VDD_CON_PWM	ADC_IN6			
2	PWM1	TPM3_CH0	FLEXIO1_FLEXIO4	CAN4_TX	LPUART6_TX	GPIO_IO04
3	PWM2	TPM3_CH1	FLEXIO1_FLEXIO20	GPIO_IO20		
4	PWM3	TPM3_CH3	FLEXIO1_FLEXIO24	GPIO_IO24		
5	PWM4	TPM4_CH0	FLEXIO1_FLEXIO5	CAN4_RX	LPUART6_RX	GPIO_IO05
6	PWM5	TPM4_CH1	FLEXIO1_FLEXIO21	GPIO_IO21		
7	PWM6	TPM5_CH0	FLEXIO1_FLEXIO6	GPIO_IO06		
8	PWM7	TPM5_CH1	FLEXIO1_FLEXIO22	CAN5_TX	LPI2C5_SDA	GPIO_IO22
9	PWM8	TPM6_CH1	FLEXIO1_FLEXIO23	CAN5_RX	LPI2C5_SCL	GPIO_IO23
10	GND					

1: measured on ADC_IN6 9: shared with the buzzer while S1 is ON

J13 I2C

JST-GH 1x4, top entry · DS-009 I2C · 3.3 V logic, 2.2 kΩ pull-ups

1	5V out	VDD_CON_I2C_5V0	
2	I2C6 SCL	I2C6_SCL	GPIO_IO03
3	I2C6 SDA	I2C6_SDA	GPIO_IO02
4	GND		

J25 AUDIO

3.5 mm 4-pole TRRS jack with insertion switch, board underside · CTIA / AHJ (tip L, ring 1 R, ring 2 GND, sleeve MIC)

J25 IO board ▸ WM8962B audio codec (SAI2 + I2C4) ▸ i.MX95 SoC

T	Left (tip)	HP_J_L	via WM8962B HPOUTL
R1	Right (ring 1)	HP_J_R	via WM8962B HPOUTR
R2	GND (ring 2)	GND	
S	Microphone (sleeve)	HP_MICIN	via WM8962B IN1L
SW	Insert detect	HP_J_D	via WM8962B GPIO3 (HP_JD)

S: bias voltage comes from the codec

J24 SPKR

JST-PH 2.0 mm 1x4

J24 IO board ▸ WM8962B audio codec (SAI2 + I2C4) ▸ i.MX95 SoC

1	Left −	SPKOUTLN	WM8962 codec
2	Left +	SPKOUTLP	WM8962 codec
3	Right −	SPKOUTRN	WM8962 codec
4	Right +	SPKOUTRP	WM8962 codec

1: not GND 3: not GND

J8 CAN2

JST-GH 1x4, side entry · DS-009 CAN

120 Ω termination: fitted

1	5V out	CON_CAN2_5V0				
2	CAN2 H	CAN2_H	CANH	TJA1463 CAN FD transceiver	TXD	CAN2 TX / GPIO_IO25
3	CAN2 L	CAN2_L	CANL		RXD	CAN2 RX / GPIO_IO27
4	GND					

J14 TELEM

JST-GH 1x6, top entry · DS-009 TELEM · 3.3 V logic

1	5V out	VDD_CON_UART_5V0	
2	UART7 TX	UART7_TX	GPIO_IO08
3	UART7 RX	UART7_RX	GPIO_IO09
4	UART7 CTS	UART7_CTS_B	GPIO_IO10
5	UART7 RTS	UART7_RTS_B	GPIO_IO11
6	GND		

J4 CAN1

JST-GH 1x4, side entry · DS-009 CAN

120 Ω termination: fitted

1	5V out	CON_CAN1_5V0				
2	CAN1 H	CAN1_H	CANH	TJA1463 CAN FD transceiver	TXD	CAN1 TX / PDM_CLK
3	CAN1 L	CAN1_L	CANL		RXD	CAN1 RX / PDM_BIT_STREAM0
4	GND					

J9 CAN3

JST-GH 1x4, side entry · DS-009 CAN

120 Ω termination: fitted

1	5V out	CON_CAN3_5V0					
2	CAN3 H	CAN3_H	CANH	TJA1463 CAN FD transceiver	TXD	74AVC4T3144 level shifter	CAN3 TX / CCM_CLKO3
3	CAN3 L	CAN3_L	CANL		RXD		CAN3 RX / CCM_CLKO4
4	GND						

PIN COLOURS — 5 V · 3.3 V · GND · UART · I2C · PWM / timer · CAN FD · GPIO / misc · Audio

J1 M.2 KEY M

M.2 Socket 3 Key M, 2242 / 2280 standoffs, 3.3 V up to 3.5 A

J1 Main board ▸ PI6C clock buffer 100 MHz REFCLK ▸ PCAL6524 I/O expander (control pins) ▸ P3H2840 I3C hub all marked pins ▸ i.MX95 SoC

PCIe x1: lane 0 only · No SATA

3V3	3.3 V ×9	VDD_3V3_M2_KEYM	
GND	GND ×11	GND	
10	Activity LED	LED_GRN	
40	SMBus CLK	M2_SMBUS_CLK	
41	PCIe RX0 −	PCIE1_RX0_N	PCIE1_RX0_N
42	SMBus DATA	M2_SMBUS_DATA	
43	PCIe RX0 +	PCIE1_RX0_P	PCIE1_RX0_P
44	SMBus ALERT#	M2_SMBUS_ALERT_B	
47	PCIe TX0 −	PCIE1_TX0_N	PCIE1_TX0_N
49	PCIe TX0 +	PCIE1_TX0_P	PCIE1_TX0_P
50	PERST#	M2_KEYM_PERST_B	
52	CLKREQ#	M2_KEYM_CLKREQ_B	
53	REFCLK −	M2_KEYM_REFCLK_N	
54	PEWAKE#	M2_KEYM_PEWAKE_B	
55	REFCLK +	M2_KEYM_REFCLK_P	
69	PEDET (card detect)	M2_KEYM_PEDET	

3V3: pins 2, 4, 12, 14, 16, 18, 70, 72, 74 GND: pins 3, 9, 15, 27, 33, 39, 45, 51, 57, 71, 73
10: drives the KEY_M_ACT LED 40: 1.8 V 47: AC coupled on the board
49: AC coupled on the board 53: 100 MHz 55: 100 MHz

J2 CONSOLE

JST-GH 1x6 (SM06B-GHS-TB) · DS-009 TELEM · 3.3 V logic

1	5V out	VDD_SYS_5V0	
2	UART1 TX	UART1_TXD/BT_MODE0	UART1_TXD
3	UART1 RX	UART1_RXD	UART1_RXD
4	UART2 RX	UART2_RXD	UART2_RXD
5	UART2 TX	UART2_TXD/BT_MODE1	UART2_TXD
6	GND		

2: Linux console; boot strap BT_MODE0
4: M7 console, on the UART1 CTS pin
5: M7 console, on the UART1 RTS pin; boot strap BT_MODE1

J7 DEBUG

2x5 1.27 mm (Samtec SHF-105-01-L-D-RA) · Arm Cortex 10-pin debug · 1.8 V logic (VTref)

VTref 1.8V	VDD_1V8	1 2	SWDIO / TMS	DEBUG_TMS_SWDIO	DAP_TMS_SWDIO
GND	GND	3 4	SWCLK / TCK	DEBUG_TCLK_SWCLK	DAP_TCLK_SWCLK
GND	GND	5 6	SWO / TDO	DEBUG_TDO_TRACESWO	DAP_TDO_TRACESWO
Key	GND	7 8	TDI	DEBUG_TDI	DAP_TDI
GNDDetect	GND	9 10	nRESET	SYS_RST_B	via PF09 PMIC / POR_B

7: tied to GND 10: open drain

J16 M.2 KEY B

M.2 Socket 2 Key B / B+M, 2242 / 3042 / 3052 standoffs, bottom side, 3.3 V up to 5 A

J16 Main board ▸ PI6C clock buffer 100 MHz REFCLK ▸ PCAL6524 I/O expander (control pins) ▸ SIM holder J5 all marked pins ▸ i.MX95 SoC

PCIe x1: lane 0 only · No USB: modem must be a PCIe model

3V3	3.3 V ×5	VDD_3V3_M2_KEYB	
GND	GND ×11	GND	
1	CONFIG_3	M2_KEYB_CONFIG3	
6	FCPO#	M2_KEYB_FCPO_B	
8	W_DISABLE1#	M2_KEYB_WDISABLE1_B	
10	Activity LED	LED_GRN	
20	GPIO_5	M2_KEYB_GPIO5	
21	CONFIG_0	M2_KEYB_CONFIG0	
22	GPIO_6	M2_KEYB_GPIO6	
23	WAKE#	M2_KEYB_WOWWAN_B	
24	GPIO_7	M2_KEYB_GPIO7	
26	W_DISABLE2#	M2_KEYB_WDISABLE2_B	
30	SIM RST	UIM_RESET	
32	SIM CLK	UIM_CLK	
34	SIM I/O	UIM_DATA	
36	SIM VCC	UIM_PWR	
41	PCIe RX0 −	PCIE2_RX0_N	PCIE2_RX0_N
43	PCIe RX0 +	PCIE2_RX0_P	PCIE2_RX0_P
47	PCIe TX0 −	PCIE2_TX0_N	PCIE2_TX0_N
49	PCIe TX0 +	PCIE2_TX0_P	PCIE2_TX0_P
50	PERST#	M2_KEYB_PERST_B	
52	CLKREQ#	M2_KEYB_CLKREQ_B	
53	REFCLK −	M2_KEYB_REFCLK_N	
54	PEWAKE#	M2_KEYB_PEWAKE_B	
55	REFCLK +	M2_KEYB_REFCLK_P	
66	SIM_DETECT		
67	RESET#	M2_KEYB_RESET_B	
69	CONFIG_1	M2_KEYB_CONFIG1	
75	CONFIG_2	M2_KEYB_CONFIG2	

3V3: pins 2, 4, 70, 72, 74 GND: pins 3, 5, 11, 27, 33, 39, 45, 51, 57, 71, 73
1: 10 kΩ pull-up 6: full card power off 10: drives the KEY_B_ACT LED 20: 1.8 V
21: 10 kΩ pull-up 22: 1.8 V 23: wake on WWAN 24: 1.8 V 36: supplied by the module
47: AC coupled on the board 49: AC coupled on the board 53: 100 MHz 55: 100 MHz
66: 10 kΩ pull-up 67: 1.8 V 69: 10 kΩ pull-up 75: 10 kΩ pull-up

J4 5V

1x3 2.54 mm right-angle header, not fitted

Not fitted

1	5V out	CON_DISP_5V0
2	GND	
3	GND	

J11 RTC_BAT

JST-SH 1.0 mm 2-pin (SM02B-SRSS-TB), top entry

J11 Main board ▸ PCF2131 RTC (I2C2, 0x53) ▸ i.MX95 SoC

1	GND	
2	Battery +	VBAT

2: charged slowly, about 3 V

J3 CSI

22-pin 0.5 mm FPC/FFC, contacts away from the PCB · RPi 22-pin CSI layout · 1.2 V MIPI, 3.3 V I2C and GPIO

J3 CAM board ▸ IP4292 MIPI ESD arrays ▸ PCA9306 I2C level shifter ▸ i.MX95 SoC

RPi camera modules fit (22-pin FFC) · RPi DSI displays: DSICSI_B2B port only

1	GND		
2	CSI D0 −	MIPI_CSI_D0_N	MIPI_CSI1_D0_N
3	CSI D0 +	MIPI_CSI_D0_P	MIPI_CSI1_D0_P
4	GND		
5	CSI D1 −	MIPI_CSI_D1_N	MIPI_CSI1_D1_N
6	CSI D1 +	MIPI_CSI_D1_P	MIPI_CSI1_D1_P
7	GND		
8	CSI CLK −	MIPI_CSI_CLK_N	MIPI_CSI1_CLK_N
9	CSI CLK +	MIPI_CSI_CLK_P	MIPI_CSI1_CLK_P
10	GND		
11	CSI D2 −	MIPI_CSI_D2_N	MIPI_CSI1_D2_N
12	CSI D2 +	MIPI_CSI_D2_P	MIPI_CSI1_D2_P
13	GND		
14	CSI D3 −	MIPI_CSI_D3_N	MIPI_CSI1_D3_N
15	CSI D3 +	MIPI_CSI_D3_P	MIPI_CSI1_D3_P
16	GND		
17	Camera GPIO 1	CAM1_IO1_CON	via I/O expander
18	Camera GPIO 2	CAM1_IO2_CON	via I/O expander
19	GND		
20	I2C SCL	SCL_3V3_CON	via PCA9306 / I3C2_SCL
21	I2C SDA	SDA_3V3_CON	via PCA9306 / I3C2_SDA
22	3.3V out	VDD_CON_3V3	

J5 SIM

SIM card holder, 6 contacts + card-detect switch, bottom side

J5 Main board ▸ M.2 Key B J16 UIM pins 30-36, 66 ▸ i.MX95 SoC

C1	VCC	UIM_PWR
C2	RST	UIM_RESET
C3	CLK	UIM_CLK
C5	GND	
C6	VPP	NC
C7	I/O	UIM_DATA
CD	Card detect	SIM_DETECT

C1: from the module CD: closes to GND

J9 PWR_IN

Molex Micro-Fit 3.0 2-pin (0430450223)

1	BATT +	VDD_BAT
2	BATT -	GND

PIN COLOURS VIN 9-52 V · 5 V · 3.3 V · GND · UART · I2C · PCIe / M.2 · SWD / JTAG · GPIO / misc · MIPI CSI · NC / key